Memristor model for simulating large circuits for massively-parallel analog computing

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Abstract. The model of memristor described in the paper is designed for building models of large networks for analog computations. A circuit containing thousands of memristors for finding the shortest path in a complicated maze is a typical example. The model is designed to meet the following criteria: 1. It is a model of HP memristor with linear dopant drift while respecting the physical bounds of the internal state variable. 2. Reliable operation in the SPICE environment also when simulating extremely large networks. 3. Minimization of the simulation time while computing bias points and during transient analyses. A benchmark circuit for testing the applications of various complexities is presented. The results confirm a perfect operation of the model also in applications containing thousands of memristors.

Keywords: memristor, model, massively-parallel analog computations, SPICE.

1 Introduction

Circuits for massively-parallel computing, when the collective cooperation of a large number of memristors results in effects unattainable by digital computers, are important potential application areas of memristors. Fast searching for paths in complicated labyrinths, when the computation time grows exponentially with the maze size, is a typical example. An interesting method for solving efficiently this problem via a memristor network is proposed in [1]. By means of analog switches, this network can be reconfigured to the form of the analyzed labyrinth. When applying DC voltage across terminals, which represent the entrance and the exit of the maze, the current flows only through the memristors which lie on the sought paths inside the labyrinth. After disconnecting the source, these paths are memorized in the form of memristances of the corresponding memristors. The path lengths can be evaluated via measuring the total resistances of individual paths. Such a principle is used in [2] for finding optimal trajectories of the passenger on the London tube network, which is modeled by a memristive grid.

Experimenting with such networks requires hundreds if not thousands of memristors. Their samples are not currently accessible. However, problems also exist with computer simulations of such large circuits. The numerical problems burdening simple models of the HP memristor with frequently used window functions [3] increase with increasing complexity of the application circuit. The experiments up to now with these models reveal their malfunction in the SPICE environment also for primitive circuits containing only one memristor. The well-known Pickett's model of TiO_2 memristor [4] is rather complicated in itself: in a SPICE implementation, suggested in [5], it represents 26 additional equations. When utilizing such a model in the application network containing 1000 memristors, then it represents additional 26 thousand rows and 26 thousand columns in the circuit matrix. In addition, the Pickett's model labors with serious convergence problems. A simple circuit can be shown, containing 8 memristors, each modeled by the Pickett's model, whose DC solution cannot be found in SPICE due to numerical problems.

The paper describes a model of the HP memristor with linear dopant drift, which is mathematically equivalent to the classical Strukov model [6], but taking into account the physical limits of the internal state variable $x \in [0,1]$, which is the normalized width of the doped (and thus conductive) TiO_2 layer [7]. This limitation is commonly modeled by a rectangular window function [7]. However, such a model fails numerically if the memristor reaches either border of the state variable. For our purposes we will therefore use the method of nonlinear transformation [3] of the native state variable (charge) into the physical state variable (x), which must be optimized in order to minimize the total count of equations for the simulation program.

2 Proposed model of HP memristor

The classical model of the TiO_2 memristor is in the form [7]

$$v = R_m(x) \cdot i\,,\ R_m(x) = R_{on}x + R_{off}(1-x) = R_{off} - \Delta R x\,, \tag{1}$$

$$\frac{dx}{dt} = kif_w(x)\,,\ k = \frac{\mu_v R_{on}}{D^2}\,. \tag{2}$$

Here v, i, and R_m are the memristor voltage, current, and resistance (memristance), R_{on} and R_{off} are the limiting values of the memristance at the boundary states $x = 1$ and $x = 0$, and $\Delta R = R_{off} - R_{on}$. The boundary speed in (2) is directly proportional to current, where k is a technological constant, dependent on the dopant mobility μ_V, on the resistance R_{on}, and on the total length D of the oxide. The window function $f_w(x)$ models the boundary phenomena, when the boundary speed in the vicinity of the states $x = 1$ and $x = 0$ is slowed down. The role of the simplest rectangular window ($f_w(x) = 0$ for $x \le 0$ and $x \ge 1$, $f_w(x) = 1$ for other x) is to stop the boundary movement in order that x does not fall outside its physical limits.

The differential equation (2) can be integrated in the form [3]

$$\int \frac{dx}{f_w(x)} = F_w(x) + C_w = k\int i dt = kq = \bar{q} \tag{3}$$

where C_w is a constant of integration, $\bar{q}$ is the normalized charge, and the primitive function $F_w(x)$ transforms the state variable x into the normalized charge. The inverse $FI_w(\bar{q})$ for the case of rectangular window and for C_W = 0 has a piece-wise linear form according to Fig. 1.

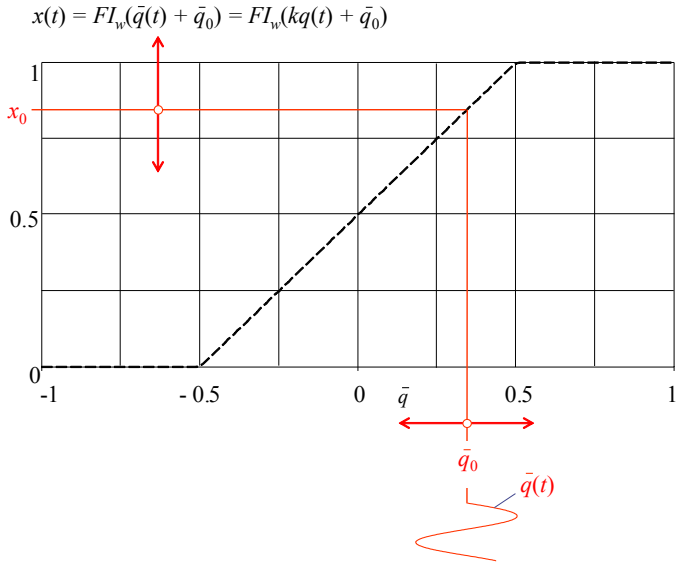

Fig. 1. Nonlinear function for transforming the normalized charge $\bar{q}$ into the normalized physical state variable x of TiO_2 memristor with rectangular window.

Instead of the differential equation (2), a simpler equation between current and charge

$$\frac{dq}{dt} = i \tag{4}$$

will be a part of the memristor model. Its numerical solution is trivial. The computed charge must then be normalized by multiplying it by the constant k from Eq. (2), and transform it subsequently into the state variable x via the nonlinear transformation according to Fig. 1. The memristance can be evaluated from x by Eq. (1). The initial state of the memristor can be defined in one of three ways: (A) As initial memristance, which is related unambiguously to the initial state x_0 via Eq. (1). (B) As initial state x_0. Its limiting values 0 and 1 correspond to the memristances R_{off} and R_{on}. (C) As initial normalized charge $\bar{q}_0$. According to Fig. 1, its values -0.5, 0.5, and 0 correspond to the x states 0, 1, and 0.5, and to the memristances R_{off}, R_{on}, and $(R_{on}+R_{off})/2$. Method (C) is most general because it enables defining the initial state of the memristor also outside the region of linearly increasing characteristic in Fig. 1.

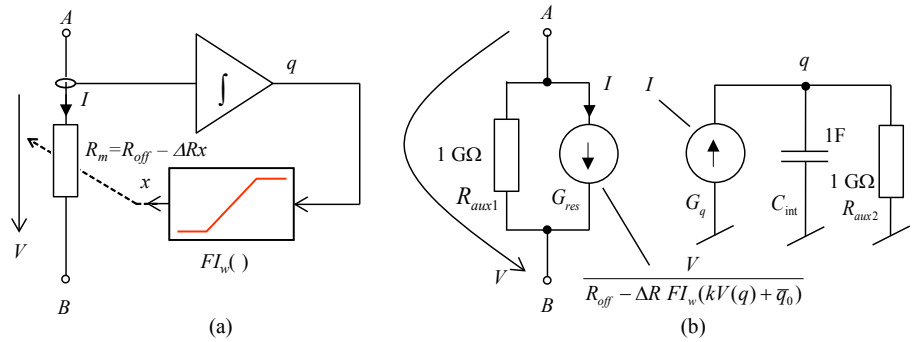

Fig. 2. Model of HP memristor, (a) ideological, (b) for SPICE implementation.

The mechanism of memristor modeling is shown in Fig. 2 (a): The memristor current is sensed and transformed into a charge via integration. The block FI_w transforms the charge into the state variable x, which controls the memristance. Figure 2 (b) represents the model for its effective implementation in SPICE. In addition to the couple of terminals A and B, only one additional node q appears in the model, whose voltage is equal to the computed charge. The memristance is modeled via the controlled current source. To avoid a potential conflict of ideal current sources in the application circuit, the A and B terminals are shunted by the auxiliary resistor R_{aux1}, whose resistance is much greater than that of R_{off}. The auxiliary resistor R_{aux2} is necessary for defining the DC path from node q to ground.

3 Benchmark circuit

The benchmark circuit in Fig. 3 consists of $2MN+M+N$ identical memristors. Its complexity can be arbitrarily varied by selecting the parameters M and N. The signal source is applied between the *in* and ground terminals. The current source has been selected for experiments described below, providing either DC current or sinusoidal waveform with adjustable amplitude, frequency and initial phase, with the voltage response being evaluated in both cases. For sinusoidal excitation, the fingerprints of v–i pinched hysteresis loops can be tested. The experiments were done in Micro-Cap 11 on a PC with Intel(R) Core(TM) i7-3770 CPU @ 3.4GHz and 16GB RAM, Windows 7 Ultimate 64 bit.

Figures 4 and 5 summarize the simulations of an extremely large circuit with M=50 and N=30, thus containing 3080 memristors. Figure 4 shows the evolution of voltage at the *in* node driven by DC 250μA current flowing into the node. All the memristors have the same initial memristances. As is obvious from the current direction, all vertical/horizontal memristors will decrease/increase their resistances. The initial resistance of the *in* node is given by the resistance of the network with identical 6 kΩ resistors, whereas the final resistance is given by the network of vertical R_{on} and horizontal R_{off} resistors. The corresponding initial and final voltages are shown in Fig. 4. The non-monotonic transient can be achieved via selecting a proper value of R_{ini}.

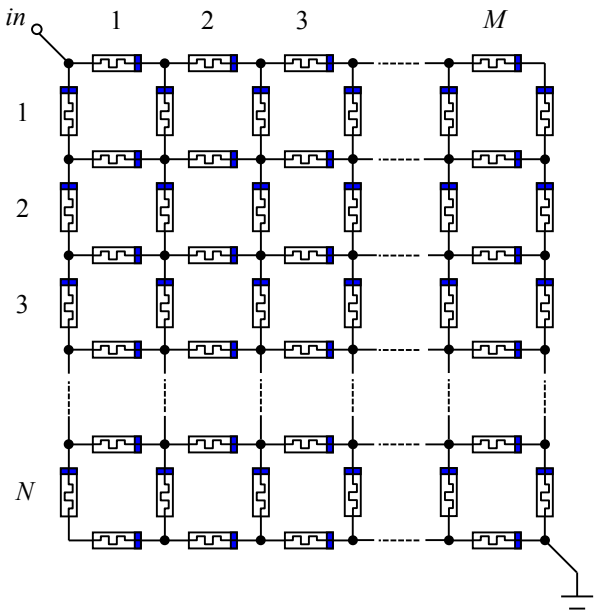

Fig. 3. Benchmark circuit compounded of $2MN+M+N$ identical memristors.

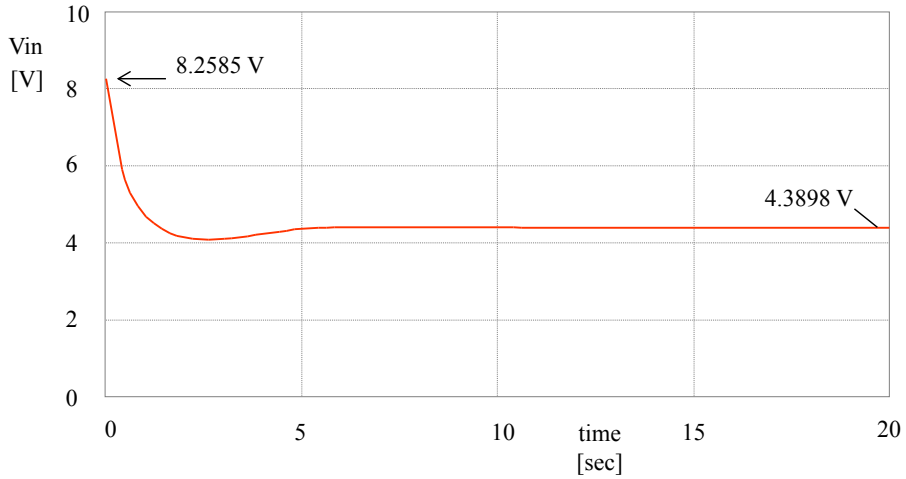

Fig. 4. Results of transient analysis of the circuit from Fig. 3 for M=50, N=30: voltage response to a constant current of 250 μA flowing into the *in* node; R_{ini} = 6 kΩ, R_{on} = 100Ω, R_{off} = 10kΩ, step ceiling = 0.2 sec.

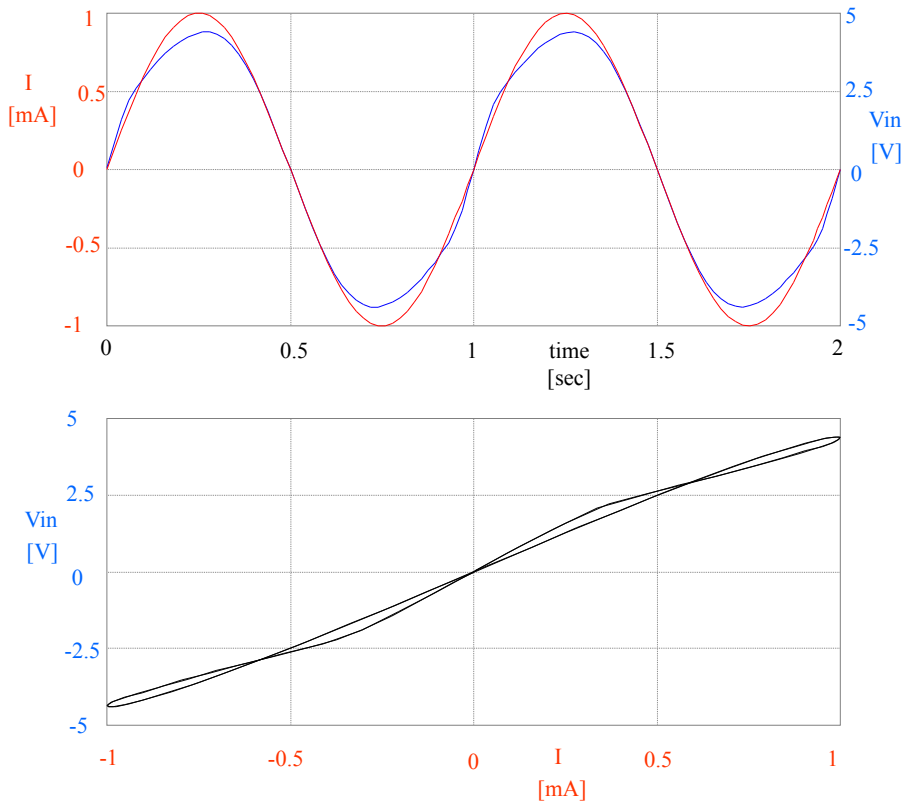

Fig. 5. Transient analysis of the circuit from Fig. 3 for M=50, N=30, driven by sinusoidal 1 mA/ 1 Hz current; R_{ini} = 1.3 kΩ, R_{on} = 100 Ω, R_{off} = 10 kΩ; step ceiling = 0.02 sec.

Figure 5 provides the simulation results of the same circuit for sinusoidal excitation. It should be noted that the pinched hysteresis loop can exhibit crossing points also outside the v–i origin. This status can be adjusted via a proper selection of the initial memristance.

The computation times for transient analyses from Figs 4 and 5 were approximately the same, ca 4 seconds. Similar analyses of more complicated circuits with M=N=50, thus containing 5100 memristors, and $M = N = 100$ with 20200 memristors take ca 9 and 40 seconds, respectively.

4 Conclusions

Computer experiments with extremely large circuits, containing the proposed model of the HP memristor, confirm the robustness of this model. It enables a fast and reliable analysis of circuits containing thousands of memristors. Comparable

parameters are absolutely unavailable for classical memristor models, irrespective of whether they utilize the window functions or the Pickett – type physical models.

In the case of the necessity of modeling the nonlinear boundary effects in the TiO_2 memristor, a sigmoidal function according to [3] can be used instead of the piece-wise-linear transforming function between native and physical state variables, with the principle of the model and its advantageous parameters remaining preserved.

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